REMARKS

Upon entry of this amendment, claims 1-4, 11-16, and 19-20 will be amended, and claims 5-10 and 17-18 will be canceled. The claims have been amended solely to expedite prosecution of the present application. No new matter has been added, and Applicant reserves the right to pursue the subject matter of the original claims in this application and in other applications. Allowance of the pending claims is respectfully requested in view of the amendments and the following remarks.

As an initial matter, the specification stands objected to for failing to provide a concise statement of the technical disclosure including that which is new in the art. Applicant has amended the Abstract in view of the Examiner's helpful suggestions.

In addition, claims 1-20 are rejected under 35 USC 112, second paragraph, as being indefinite because the terms "higher-quality" and "lower-quality" might refer to any characteristic of a material. These terms have been removed from the independent claims. Moreover, claims 11 and 18 are rejected as being indefinite because of the terms "more homogeneous" and "less homogeneous."

Claim 2 now recites that a second material "is substantially more dielectric" than a first material. Applicants respectfully submit that all of the pending claims, together with the discussion in the Specification at page 4, lines 1-19, would be understood by those of ordinary skill in the art of printed circuit board design as particularly pointing out and distinctly claiming the subject matter which Applicant regards as his invention. Applicants therefore request that the 112 rejections be withdrawn.

Claims 1-20 are rejected under 35 U.S.C. 102 as being anticipated by US Patent No. 4,949,224 ("Yamamura"). As amended, all of the claims are directed to an embodiment such as, for example, the ones illustrated in FIG. 3 of the present application. That is, a first integrated circuit is attached to both a first printed circuit board and a second printed circuit board (by being integrated into solderjoint interfaces between the first integrated circuit and the first board). Moreover, a second integrated circuit, remote from the first integrated circuit, is similarly attached to both boards.

Applicants note that in FIG. 4 of Yamamura, <u>no</u> signal contacts of the chip 21 are attached to the circuit board 23 via a solderjoint interface as recited in the pending claims. Yamamura also does not disclose <u>remotely</u> located integrated circuits as recited in the pending claims (*e.g.*, FIGS. 1 and 3 of Yamamura disclose co-located semiconductor devices 10a, 10b). Nor would either of these features be obvious in view of this reference.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-0191.

Respectfully submitted,

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